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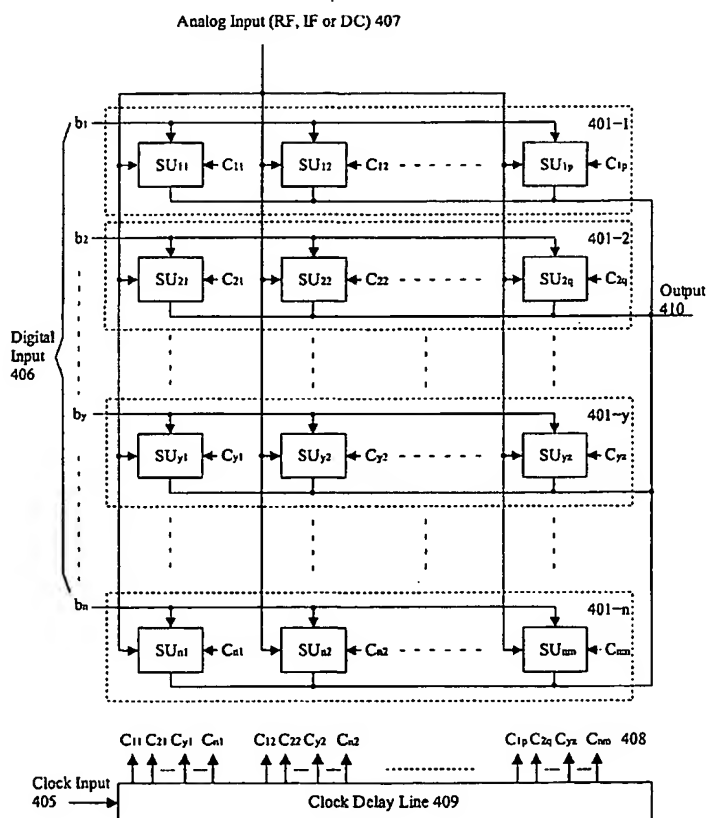
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[Continued on next page]

(54) Title: A DIRECT DIGITAL AMPLITUDE MODULATOR



(57) Abstract: This invention provides various embodiments of a direct digital amplitude modulator (DDAM) for modulating radio frequency (RF) or intermediate frequency (IF) or baseband signal with the invented interpolation technique. The interpolation technique greatly reduces the amplitudes of alias signals without using an analog filter. The invention therefore is significant for various communication transmitters to achieve simple structure, good linearity and high power efficiency.

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A DIRECT DIGITAL AMPLITUDE MODULATOR

TECHNICAL FIELD

The invention relates generally to communication transmitters requiring amplitude modulation. Modern communication systems, such as cable, cellular and satellite communications, employ non-constant envelop digital modulation to increase spectral efficiency, such as quadrature phase-shift keying (QPSK), offset QPSK (OQPSK) and quadrature amplitude modulation (QAM) etc. To transmit a non-constant envelop signal, a linear power amplifier is required in the transmitter which usually has a low power efficiency and insufficient linearity. A direct digital amplitude modulator is of great interest for a transmitter to achieve simple structure, good linearity and high power efficiency in various communication systems.

BACKGROUND OF THE INVENTION

Fig. 1 and Fig. 2 are the block diagrams of an exemplary QAM modulator. In Fig. 1, input data 100 is split into digital in-phase (I) signal 102a and quadrature (Q) signal 102b through digital signal processing (DSP) unit 101. Digital-to-analog converters (DACs) 103a and 103b are used to convert I signal 102a and Q signal 102b to analog signals, and low pass filters 104a and 104b are used to clear the alias components of the DAC outputs. In amplitude modulators 105a and 105b, the outputs of low pass filters 104a and 104b modulate carrier signals 106a and 106b which phases are separated in 90 degrees. The outputs of modulators 105a and 105b are combined in combiner 107, and the output of combiner 107 is amplified through linear power amplifier 108.

The polar modulation technique is shown in Fig. 2. Data 200 is split into digital amplitude signal 202a and phase signal 202b by DSP unit 201. Digital amplitude signal 202a is converted to analog amplitude signal through DAC 203, and low pass filter 205 clears the alias components of the DAC output. Digital phase signal 202b modulates input carrier 207 in phase modulator 204, and modulated carrier signal 206b is amplified through power amplifier 208. The gain of power amplifier 208 is linearly controlled by analog amplitude signal 206a. The embodiment in Fig. 2 is more power efficient than that

in Fig. 1, as the modulated carrier signal is a constant envelop signal, a nonlinear power amplifier can be used.

Fig. 3a shows a conventional DAC 301 with an analog reconstruction filter 302, and the spectra of digital input signal 300 and analog output signal 303 are showed in Fig. 3b and Fig. 3c respectively. From Figures 3b and 3c, when a broadband signal is transmitted, it is difficult to filter out the alias signals of the DAC output, and the wanted signal is distorted due to the DAC's non-flat sinc response. As the clock frequency (f_s) increases, the attenuation of the alias signal is increased, and the distortion of the signal is reduced.

The embodiments in Fig. 1 and Fig. 2 are not suitable for full system integration, especially in broadband data transmission. Due to the limitation of clock frequency (f_s), they need complex analog reconstruction filters to remove alias signals. The analog reconstruction filter may even need discrete components.

In mobile communications, a high efficiency power amplifier (PA) is essential, because the PA dominates the power consumption of the portable system. RF power amplifiers are most efficient when they work in switching mode and amplify a constant envelop signal. The amplification of a non-constant envelop signal requires a linear PA which is inherently less power efficient.

SUMMARY OF THE INVENTION

The objective of the present invention is to provide a direct digital amplitude modulator (DDAM) for non-constant envelop modulation. It will be easily integrated with other parts of a transmitter system to achieve a fully digitized transmitter with simple structure, good linearity, high power efficiency and low requirement on the output filter.

BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 illustrates a conventional I-Q quadrature modulator.

Fig. 2 illustrates a conventional polar modulator.

Fig. 3 illustrates a conventional DAC, its digital input and analog output spectra.

Fig. 4 shows, in the form of a block diagram, the principal and the detail of the invented
5 direct digital amplitude modulator (DDAM).

Fig. 5a shows the first embodiment of a sub-switched current source unit in this invention.

10 Fig. 5b shows an extension of the first embodiment of a sub-switched current source unit in this invention.

Fig. 6 shows the second embodiment of a sub-switched current source unit in this invention.

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Fig. 7 shows an I-Q quadrature amplitude modulator based on this invention.

Fig. 8 shows the first embodiment of a polar modulator based on this invention.

20 Fig. 9 shows the second embodiment of a polar modulator based on this invention.

DESCRIPTION OF THE INVENTION

The preferred embodiments of the present invention and its advantages are best understood by referring to Fig. 1- Fig. 9 of the drawings.

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Referring to Fig. 4, the block diagram of the direct digital amplitude modulator (DDAM) according to the present invention is shown. The n-bit digital amplitude input signal 406 controls the binary-weight switched RF, IF or DC current sources 401-1, 401-2, ..., 401-n. The binary-weight switched current source in each bit is divided into sub-switched
30 current source units (SUs). In the least significant bit (LSB) b_1 , it is divided into p sub-switched current source units SU_{11} , SU_{12} , ..., SU_{1p} . In an arbitrary bit b_y , it is divided

into z sub-switched current source units $SU_{y1}, SU_{y2}, \dots, SU_{yz}$. In the most significant bit (MSB) b_n , it is divided into m sub-switched current source units $SU_{n1}, SU_{n2}, \dots, SU_{nm}$. The numbers of sub-switched current source units in different bits can be equal or different, depending on the minimum size available in the technology and/or the density of interpolation. The sizes of SUs in each bit can be equal or different, depending on the type of interpolation.

Clock signal 405 which is synchronized with digital input 406 and has a frequency f_s , is divided into a number of delayed clock signals 408 with delays in one period of digital input 406 through clock delay line 409. For an arbitrary bit b_y , there are z delayed clock signals, and the intervals between these clock signals are equal in the normal case but can be unequal if necessary. The effective clock frequency of b_y is therefore increased to zf_s . If m/z is set to an integer, clock delay line 409 is simplified, but it is not compulsory. In the case of linear interpolation, the current sources are divided into equal size SUs in each bit. In other cases, it can be divided into different sizes according to the selected interpolation function. Analog input signal 407 to the sub-switched current source units can be an RF, IF or DC signal. When the input signal is RF or IF, output 410 is an amplitude modulated RF or IF signal. When the input signal is DC, output 410 is an amplitude modulated baseband signal. Because of the higher effective clock frequency and the interpolation function, the DDAM's alias signal's attenuation is increased, and the requirement on the output analog filter is alleviated. With an RC charge and discharge hold (RCH) circuit which will be explained in the description of Fig. 5a, the alias signals' attenuation is further increased.

Fig. 5a shows the first embodiment of the sub-switched current source units when the analog input is an RF or IF signal. Data signal 501 is obtained from DDAM's digital input signal 406, and clock signal 502 is obtained from clock delay line 409 in the DDAM. Data and clock signals 501 and 502 are sent to register 512 to produce output signal 503a and inverse output signal 503b. Transistors M_4 510 and M_5 511, controlled by output signal 503a and inverse output signal 503b of register 512 respectively, act as switches to current source transistor M_3 509. The dimensions of transistors M_4 510 and

M₅ 511 can be properly selected in order to set the switching time constant together with the parasitic capacitance to obtain a hold character somewhere between zero-order-hold and first-order-hold. The RC charge and discharge hold (RCH) character can achieve higher attenuation for the alias signals. The differential RF or IF signals are fed to transistors M₁ 508a and M₂ 508b. The power supply is provided via two loads Load₁ 513a and Load₂ 513b (not include in each sub-switched current source unit) which can be active or passive, on-chip or off-chip. Differential RF or IF output 506a and 506b are obtained from the drains of transistors M₁ 508a and M₂ 508b, and either of them can be a single-ended output. Transistors M₁ 508a and M₂ 508b can be separated from sub-switched current source unit and combined with other components.

Fig. 5b shows an extension of the first embodiment of the sub-switched current source units which realize a carrier suppressed DDAM. It uses two of the first embodiments in Fig. 5a, where signals 501, 502, 503a, 503b, 504 and register 512 are shared. Transistors M₅ 510a and M₁₀ 511b, M₆ 510b and M₉ 511a are controlled by output signal 503a and inverse output signal 503b of register 512 respectively. The differential RF or IF signals are fed to transistors M₁ 508a and M₄ 508d, M₂ 508b and M₃ 508c respectively. The drains of transistors M₁ 508a and M₃ 508c are connected together, and the drains of transistors M₂ 508b and M₄ 508d are connected together. The power supply is provided via loads Load₁ 513a and Load₂ 513b (not include in each sub-switched current source unit) which can be active or passive, on-chip or off-chip. Transistors M₁ 508a, M₂ 508b, M₃ 508c and M₄ 508d can be separated from sub-switched current source unit and combined with other components.

Fig. 6 shows the second embodiment of the sub-switched current source units when the analog input is a DC signal (i.e. the DC power supply). Data signal 601 is obtained from DDAM's digital input 406, and clock signal 602 is obtained from clock delay line 409 in the DDAM. They are sent to register 603. Output 604a and inverse output 604b of register 603 are sent to two switching transistors M₁ 607a and M₂ 607b. Bias signal 605 controls the bias of current source transistor M₃ 606. Load₁ 608a and Load₂ 608b (not include in each sub-switched current source unit) connected to power supply 610 are the

loads of switching transistors M_1 607a and M_2 607b respectively, which can be active or passive, on-chip or off-chip. Differential baseband outputs 609a and 609b are obtained from the drains of switching transistors M_1 607a and M_2 607b, and either of them can be a single-ended output.

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Fig. 7 shows a quadrature modulator for RF or IF carrier signal based on this invention. Data 701 to be transmitted is split into digital I signal and Q signal by DSP unit 702. In DDAMs 703a and 703b, the I and Q signals modulate carrier input signals 704a and 704b which phases are separated in 90 degrees. Input clock 707 is used by DSP unit 702 and DDAMs 703a and 703b. The DDAM's outputs are combined in combiner 705 to produce a digitally modulated non-constant envelop signal 706. Most alias signals are attenuated by the DDAM's transfer function.

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The polar modulation technique based on this invention is shown in Fig. 8. Data 801 is split into digital amplitude and phase signals 803 and 804 respectively through DSP 802. Digital phase signal 804 modulates the phase of the input carrier signal 806 and produces a phase modulated constant envelope signal 807 fed to the analog input of DDAM 808. Input clock 810 is used by DSP unit 802 and DDAM 808. Through DDAM 808, digital amplitude signal 803 modulates the amplitude of signal 807 to produce a digitally modulated non-constant envelop signal 809 in which the alias signals are greatly reduced.

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Instead of modulating RF and IF carrier signals directly, the invented DDAM can be used to control the bias voltage or current of an RF or IF power amplifier to produce a non-constant envelop digitally modulated signal with reduced alias components. Fig. 9 shows such an embodiment. In Fig. 9, DSP unit 902 splits input data 901 into digital amplitude signal 903 and digital phase signal 904. Digital phase signal 904 modulates RF or IF input carrier signal 910 in phase modulator 909. The phase modulated constant envelope RF or IF signal 913 is amplified in a variable gain power amplifier 907. The gain of the variable gain power amplifier is linearly controlled by bias signal 906. Digital amplitude signal 903 from DSP unit 902 is fed to the digital input of DDAM 905 to produce a baseband bias signal 906 with reduced alias components. The output of DDAM 905

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controls the gain of amplifier 907 to produce a digitally modulated non-constant envelop
RF or IF signal 908 with reduced alias components. When DSP unit 902 and phase
modulator 909 are removed, this embodiment can be used as an amplitude modulator. In
this case, signal 903 and signal 913 are replaced by Data 901 and RF or IF 910
5 respectively.

The proposed invention provides solutions for digitized transmitters. Although preferred
embodiments of the present invention have been illustrated in the accompanying
drawings and described in the foregoing detailed descriptions, various modifications may
10 be made without departing from the spirit or scope of the general invented concept as
defined by the appended claims and their equivalents.

CLAIMS

1. A direct digital amplitude modulator (DDAM) for generating an amplitude modulated signal; and it comprising:
- 5 an n-bit digital input with n parallel inputs, an analog input, a clock input and an output; and
- an n-bit digital input signal fed to the n-bit digital input for direct digital amplitude modulation; and
- an analog input signal fed to the analog input to be modulated which can be an RF, IF
- 10 or DC signal; and
- a clock input signal fed to the clock input synchronized with the digital input signal; and
- a clock delay line to produce delayed clock signals from the clock input signal with equal or unequal intervals in one period of the digital input signal; and
- 15 a number of sub-switched current source units to be switched on or off according to the combinations of the digital input signal and the delayed clock signals to produce or to cancel quantized RF, IF or DC currents and/or voltages at the times precisely controlled by the delayed clock signals respectively; and
- a circuitry to combine the outputs of the sub-switched current source units, and in the simplest case the outputs of sub-switched current source units are just connected
- 20 together to the output; and
- the said sub-switched current source units are grouped into n groups controlled by n-bit digital input signals respectively; and
- the values of currents and/or voltages generated by the said groups calculated by the lumped current and/or voltage values of the sub-switched current source units in
- 25 every groups have binary weights in normal case but can be other weights if necessary; and
- the values of currents and/or voltages generated by the said sub-switched current source units in each group can be equal in the case of linear interpolation or unequal
- 30 in the case of nonlinear interpolation depending on the interpolation function; and

the effective clock frequency of the DDAM can be greatly increased by the above arrangement when the number of sub-switched current source units and also the number of delayed clocks increases to reduce alias signal components.

- 5 2. A quadrature modulator according to Claim 1; and it comprising:
a digital signal processing unit with one data input, one clock input and two digital
outputs; and
two DDAMs according to Claim 1; and
a combiner with two inputs and one output; and
10 an digital input signal fed to the data input of the digital signal processing unit; and
a clock input signal, synchronized with the digital input signal, fed to the clock input
of the digital signal processing unit and the clock inputs of the two DDAMs according
to Claim 1 simultaneously; and
two analog input signals which phases are separated in 90 degrees fed to the analog
15 inputs of two DDAMs respectively according to Claim 1; and
the digital signal processing unit splits the digital input signal into I digital signal and
Q digital signal fed to the digital inputs of two DDAMs according to Claim 1
respectively; and
the outputs of two DDAMs according to Claim 1 are fed to the two inputs of the
20 combiner; and
an quadrature modulated signal is obtained from the output of the combiner.
3. A first embodiment of a polar modulator according to Claim 1, and it comprising:
a digital signal processing unit with one data input, one clock input and two digital
25 outputs; and
a DDAM according to Claim 1; and
a phase modulator with one digital input, one analog input and one analog output; and
an digital input signal fed to the data input of the digital signal processing unit; and
an analog input signal fed to the analog input of the phase modulator; and

a clock input signal, synchronized with the digital input signal, fed to the clock input of the digital signal processing unit and the clock input of the DDAM according to Claim 1 simultaneously; and
the digital signal processing unit splits the digital input signal into an digital
5 amplitude signal fed to the digital input of the DDAM according to Claim 1 and an digital phase signal fed to the digital input of the phase modulator; and
the analog output of the phase modulator which is a phase modulated constant envelop signal is fed to the analog input of the DDAM according to Claim 1; and
a polar modulated signal is obtained from the output of the DDAM according to
10 Claim 1.

4. A second embodiment of a polar modulator according to Claim 1; and it comprising a digital signal processing unit with one data input, one clock input and two digital outputs; and
15 a DDAM according to Claim 1; and
a phase modulator with one digital input, one analog input and one analog output; and
an analog power amplifier with one carrier input, one bias input and one output; and
an digital input signal fed to the data input of the digital signal processing unit; and
an analog input signal fed to the analog input of the phase modulator; and
20 a clock input signal, synchronized with the digital input signal, fed to the clock input of the digital signal processing unit and the clock input of the DDAM according to Claim 1 simultaneously; and
the digital signal processing unit splits the digital input signal into an digital amplitude signal fed to the digital input of the DDAM according to Claim 1 and an
25 digital phase signal fed to the digital input of the phase modulator; and
the analog output of the phase modulator which is a phase modulated constant envelop signal is fed to the carrier input of the analog power amplifier; and
the output of the DDAM according to Claim 1 is fed to the bias input of the analog power amplifier; and
30 a polar modulated signal is obtained from the output of the power amplifier.

5. A first embodiment of the sub-switched current source unit according to Claim 1; and it comprising:

a register with one data input, one clock input, one data output and one inverse data output; and

5 n-MOS transistors M_1 , M_2 , M_3 , M_4 and M_5 with the sources of M_1 and M_2 and the drain of M_3 connected together, with the gate of M_3 and the drains of M_4 and M_5 connected together, and with the sources of M_3 and M_5 grounded; and

an analog input signal and an inverse analog input signal, which can be differential RF or IF signals, are fed to the gates of M_1 and M_2 respectively; and two loads $Load_1$ and $Load_2$, which are not include in each sub-switched current source unit, with both
10 end 1 of $Load_1$ and end 1 of $Load_2$ connected to power supply, with end 2 of $Load_1$ connected to the drain of M_1 , and with end 2 of $Load_2$ connected to the drain of M_2 ; and

a digital data input signal and a clock input signal connected to the data input and the
15 clock input of the register respectively; and

the data output of the register is connected to the gate of M_4 and the inverse data output of the register is connected to the gate of M_5 ; and

a bias input signal is connected to the source of M_4 ; and

differential analog outputs are obtained from the drains of M_1 and M_2 , and either of
20 them can be a single-ended analog output; and

the dimensions of transistors M_4 and M_5 can be properly selected in order to set the switching time constant together with the parasitic capacitance to obtain a hold character somewhere between zero-order-hold and first-order-hold to achieve a higher attenuation for the alias signals; and

25 transistors M_1 and M_2 can be separated from sub-switched current source unit and combined with other components.

this structure can be realized by bipolar or other types of transistors as well, when p-MOS transistors are used, the structure of this embodiment is flipped complementarily.

6. A second embodiment of the sub-switched current source unit according to Claim 1; and it comprising:

a register with one data input, one clock input, one data output and one inverse data output; and

5 n-MOS transistors M_1 , M_2 and M_3 with the sources of M_1 and M_2 and the drain of M_3 connected together, and with the source of M_3 grounded; and

two loads $Load_1$ and $Load_2$, which are not include in each sub-switched current source unit, with both end 1 of $Load_1$ and end 1 of $Load_2$ connected to power supply, with end 2 of $Load_1$ connected to the drain of M_1 , and with end 2 of $Load_2$ connected to the
10 drain of M_2 respectively; and

a digital data input signal and a clock input signal connected to the data input and the clock input of the register respectively; and

the data output and the inverse data output of the register are connected to the gate of M_1 and the gate of M_2 respectively; and

15 a bias input signal is connected to the gate of M_3 ; and

differential analog outputs are obtained from the drains of M_1 and M_2 , and either of them can be a single-ended analog output.

this structure can be realized by bipolar or other types of transistors as well, when p-MOS transistors are used, the structure of this embodiment is flipped

20 complementarily.

7. An extension of the first embodiment of the sub-switched current source unit according to Claim 1 and Claim 5; and it comprising:

a register with one data input, one clock input, one data output and one inverse data
25 output; and

n-MOS transistors M_1 , M_2 , M_3 , M_4 , M_5 , M_6 , M_7 , M_8 , M_9 and M_{10} with the sources of M_1 and M_2 and the drain of M_7 connected together, the sources of M_3 and M_4 and the drain of M_8 connected together, with the gate of M_7 , the drains of M_5 and M_9 connected together, and with the sources of M_7 and M_9 grounded, with the gate of M_8
30 and the drains of M_6 and M_{10} connected together, and with the sources of M_8 and M_{10} grounded, and with the sources of M_5 and M_6 connected together, with the gates of

M_1 and M_4 connected together, with the gates of M_2 and M_3 connected together, with the gates of M_5 and M_{10} connected together, with the gates of M_6 and M_9 connected together, with the drains of M_1 and M_3 connected together, with the drains of M_2 and M_4 connected together; and

5 an analog input signal is fed to the gates of M_1 and M_4 , and an inverse analog input signal is fed to the gates of M_2 and M_3 , the analog input signal and the inverse analog input signal can be differential RF or IF signals; and

two loads $Load_1$ and $Load_2$, which are not include in each sub-switched current source unit, with both end 1 of $Load_1$ and end 1 of $Load_2$ connected to power supply, with

10 end 2 of $Load_1$ connected to the drains of M_1 and M_3 , and with end 2 of $Load_2$ connected to the drains of M_2 and M_4 ; and

a digital data input signal and a clock input signal connected to the data input and the clock input of the register respectively; and

the data output of the register is connected to the gates of M_5 and M_{10} , the inverse data

15 output of the register is connected to the gates of M_6 and M_9 ; and

a bias input signal is connected to the sources of M_5 and M_6 ; and

differential analog outputs are obtained from end 2 of $Load_1$ and end 2 of $Load_2$, and either of them can be a single-ended analog output; and

the dimensions of transistors M_5 and M_6 , M_9 and M_{10} can be properly selected

20 respectively in order to set the switching time constant together with the parasitic capacitance to obtain a hold character somewhere between zero-order-hold and first-order-hold to achieve a higher attenuation for the alias signals.

this structure can be realized by bipolar or other types of transistors as well, when p-MOS transistors are used, the structure of this embodiment is flipped

25 complementarily.

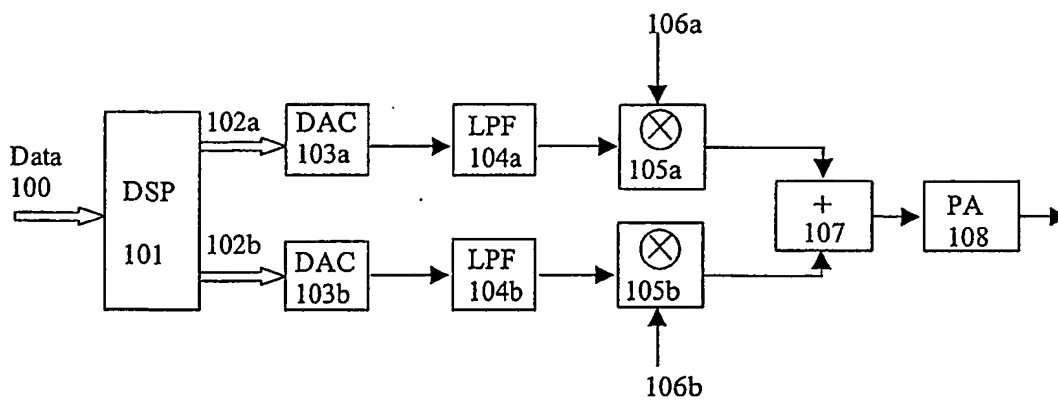


Fig. 1 Prior Art 1.

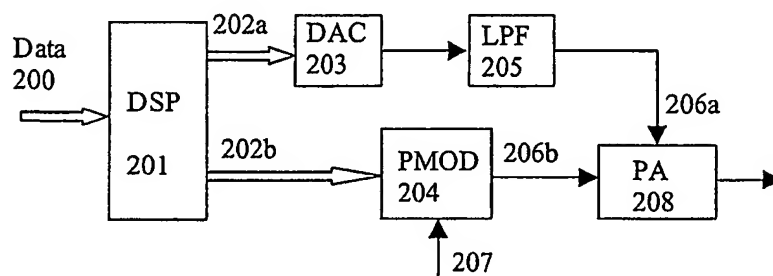


Fig. 2 Prior Art 2.

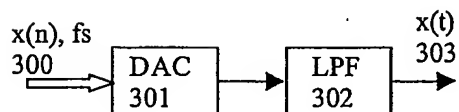


Fig. 3a Prior Art 3.

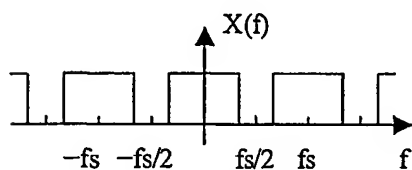


Fig. 3b

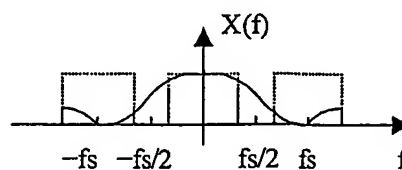


Fig. 3c

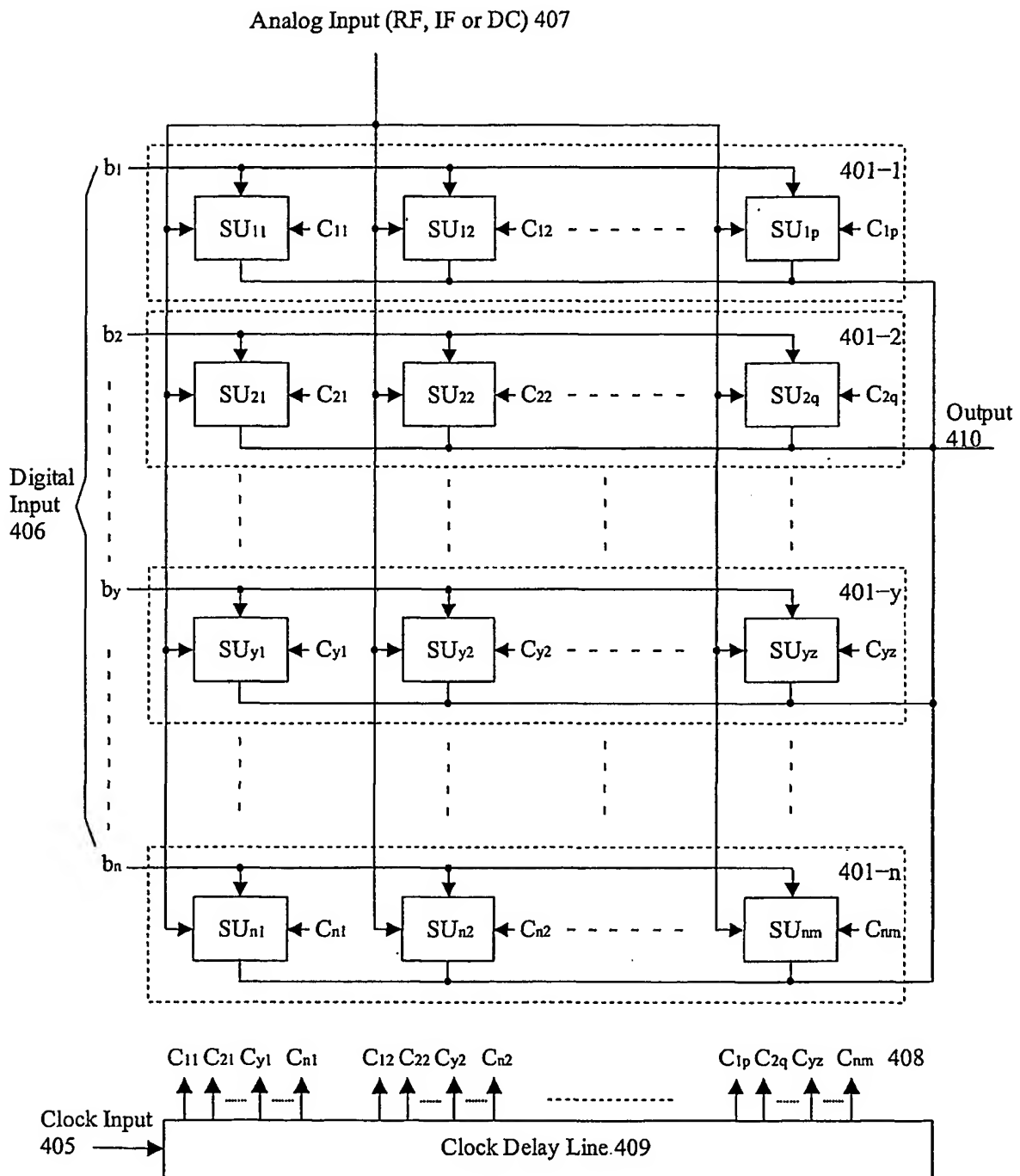


Fig. 4

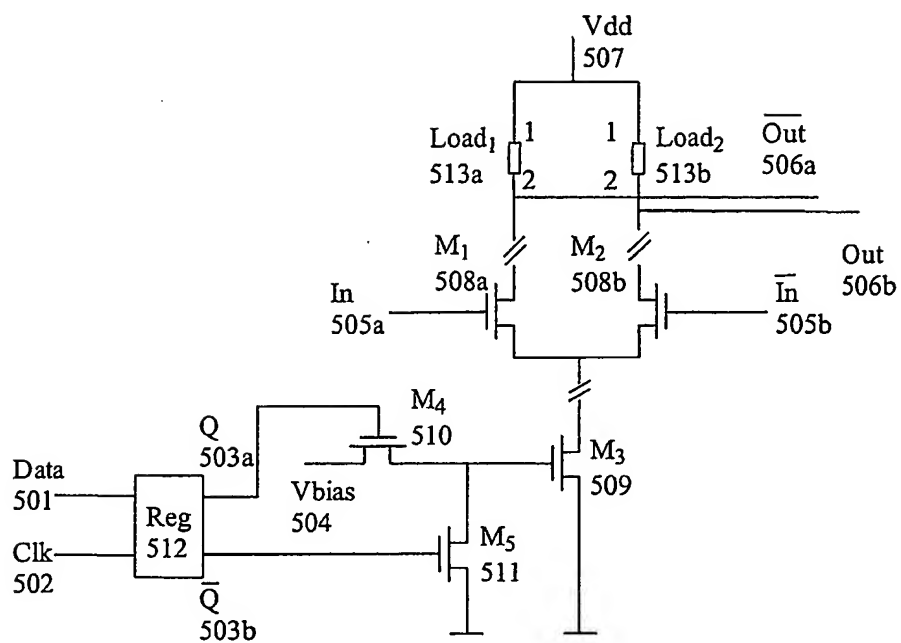


Fig. 5a

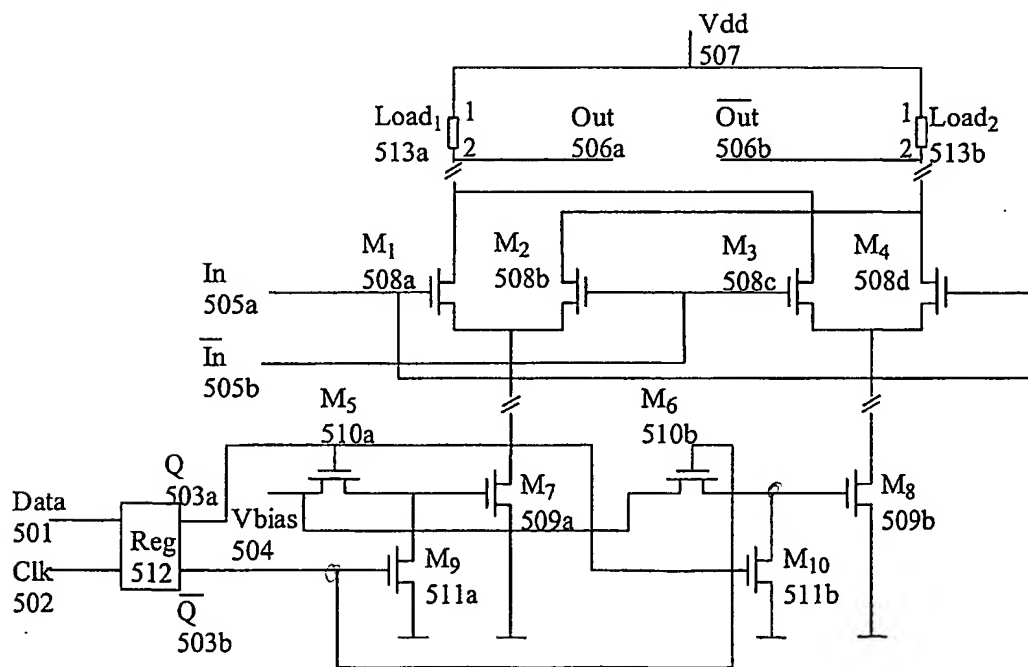


Fig. 5b

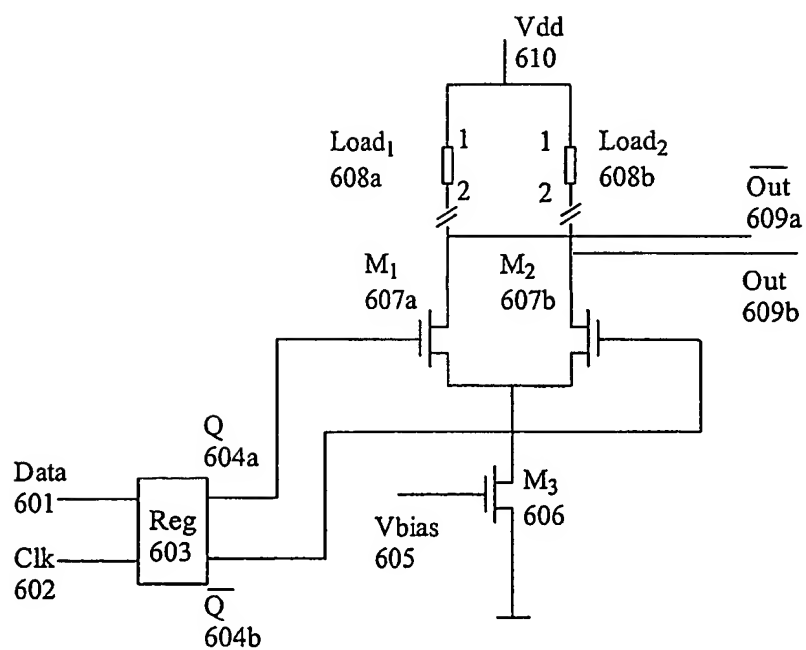


Fig. 6

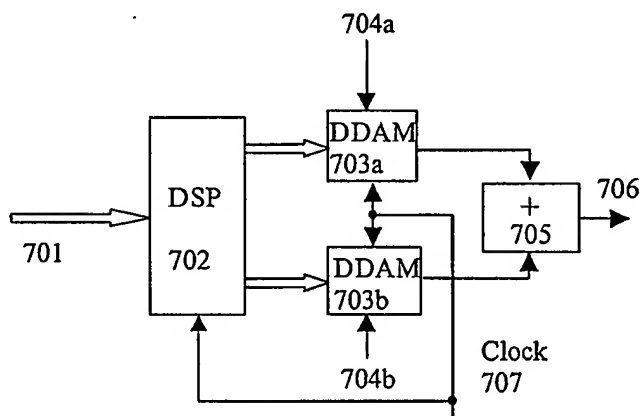


Fig. 7

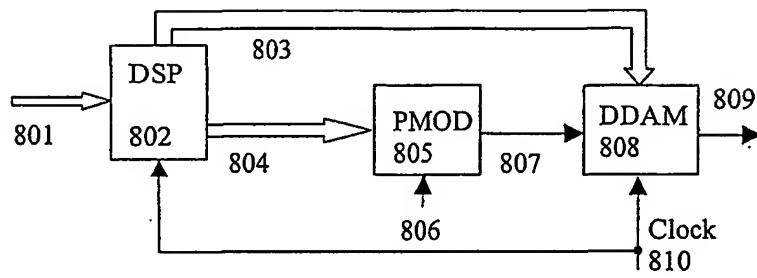


Fig. 8

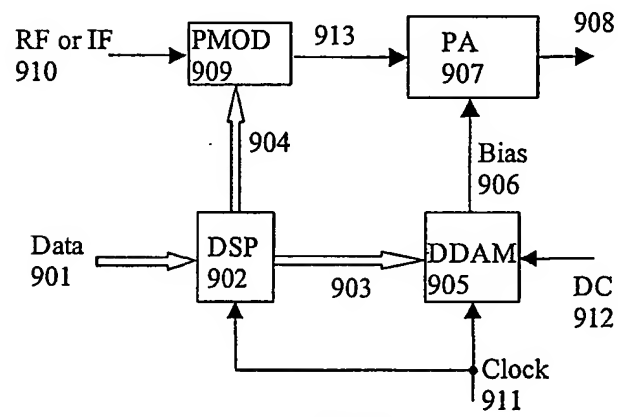


Fig. 9

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SE 01/02411

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H03C 1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H03C, H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL, WPI-DATA, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,A	The 2 International Symposium on Circuits and Systems, 2001.ISCAS 2001, pages 116-119 vol 4, 6-9 May 2001, ISBN: 0-7803-6685-9, Yijun Zhou et al: "An 8-Bit, 100-MHz low glitch interpolation DAC", see the whole document --	1-7
A	WO 9911040 A1 (NOKIA TELECOMMUNICATIONS OY), 4 March 1999 (04.03.99), abstract --	1-7
A	WO 9952206 A1 (ERICSSON, INC.), 14 October 1999 (14.10.99), abstract --	1-7

☒ Further documents are listed in the continuation of Box C.
 ☒ See patent family annex.

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/SE 01/02411

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT
Information on patent family members

27/12/02

International application No.
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